EFFICIENT VEDIC MULTIPLIER

SONALI BHOSALE & VRUSHALI RAUT

Sinhgad College of Engineering, Pune, Maharashtra, India

ABSTRACT

Multiplier is one important block in the digital signal processor, computer. There are various multiplier architectures are present, but in that simple multiplication is done using vedic mathematics through vedic multiplier. Vedic multiplier uses vedic mathematics such as Urdhva Triyakbhyam and Nikhilam sutra. Using that multiplier we have low power consumption, low delay and high speed. Which has become one of the important key area in VLSI design using CMOS challenging technology.

KEYWORDS: Multiplier, Wallace Tree, Vedic Multiplier, Nikhilam and Urdhva Triyakbhyam Formula, CMOS Layout Technology